Remarks

The final Office Action dated February 13, 2008 lists the following rejection: claims 1-2, 4, 6-12 and 14-16 stand rejected under 35 U.S.C. § 103(a) over Mori *et al.* (U.S. Patent Pub. 2002/0093073) in view of Nakamura (U.S. Patent No. 6,222,225). Claims 3, 5 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

Applicant respectfully traverses the § 103(a) rejection of claims 11-12 and 14-16 because the cited combination does not correspond to the claimed invention which includes, for example, aspects directed to partially removing the isolation zones to completely expose the side walls of the second layer of floating gate material and to partially expose the side walls of the first layer of floating gate material. The Examiner has not asserted that the Mori or Nakamura reference teach these aspects of the claimed invention. Applicant submits that the cited portions of the Mori reference do not teach partially removing isolation regions 21-24 to completely expose the side walls of second and third conductors 51-56 or partially removing isolation regions 21-24 to partially expose the side walls of first conductors 41-43. *See, e.g.,* Figure 8. Applicant further submits that the cited portions of the Nakamura reference do not address these deficiencies of Mori. Thus, the cited combination does not correspond to the claimed invention. Applicant notes that similar aspects directed to partially removing the isolation zones are found in claim 3, which is indicated by the Examiner as being allowable over the Mori and Nakamura references. Thus, it is unclear to Applicant why the Examiner has rejected claims 11-12 and 14-16 over the same references. Accordingly, the § 103(a) rejection of claims 11-12 and 14-16 is improper and Applicant requests that it be withdrawn

Applicant respectfully traverses the § 103(a) rejection of claims 1-2, 4, 6-12 and 14-16 because the modification of the Mori reference proposed by the Examiner defeats a stated purpose of Mori. According to M.P.E.P. § 2143.01, if a "proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *See, also In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984). The Examiner proposes to modify Mori such that the second and third conductors 51-56 completely fill trenches 11. *See,*

e.g., Figures 3C, 4A and 4B. Applicant submits that the Examiner's modification would defeat Mori's purpose of increasing the capacitive coupling between the floating gates (42, 53, and 54) and control gate 7. *See, e.g.*, Paragraph 0047. Mori teaches that the capacitive coupling between the floating gates (42, 53, and 54) and control gate 7 is increased by increasing the side face areas of the second and third conductors 53-54. The Examiner's proposed modification would result in the elimination of these side face areas by completely filling the trench 11 with conductor film 5, thereby reducing the capacitive coupling between the floating gates (42, 53, and 54) and control gate 7. As such, there would be no motivation for the skilled artisan to modify Mori in the manner proposed by the Examiner. Accordingly, the § 103(a) rejection of 1-2, 4, 6-12 and 14-16 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 103(a) rejection of claims 1-2, 4, 6-12 and 14-16 because the Examiner has not provided any evidence of motivation to combine the Mori and Nakamura references. This approach is contrary to the requirements of § 103 and relevant law. *See, e.g., KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007) ("A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art."). In this instance, the Examiner asserts that it would be obvious to modify Mori to completely fill the trench 11 with the second layer of floating gate material "because depositing the second floating gate material is not only limited to partially filling the cavity, but completely filling the cavity can obviously be preformed to obtain a semiconductor memory device." The Examiner appears to be asserting that the skilled artisan would completely fill the trenches 11 with the second layer of floating gate material simply because one could completely fill the trenches 11. Thus, the Examiner has merely asserted that the skilled artisan could do something without providing any reason why the skilled artisan would. Applicant submits that the Examiner has simply identified elements and appears to be improperly arranging these elements in the manner taught by Applicant's disclosure. *See, e.g.*, M.P.E.P. § 2145. Accordingly, the Examiner has not provided any evidence as to why one of skill in the art would find the asserted combination obvious as required. *See, e.g.*, M.P.E.P. § 2142. Therefore, the § 103(a) rejection of 1-2, 4, 6-12 and 14-16 is improper and Applicant requests that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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